

ABSTRACT

[045] A method and system is disclosed for inserting dummy metal into a circuit design, which includes a plurality of objects and clock nets. Aspects of the invention include identifying free spaces on each layer of the chip design suitable for dummy metal insertion, wherein the free spaces are referred to as dummy regions. Thereafter, the dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last. In a preferred embodiment, the dummy regions are further prioritized such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.